IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2823
Examiner: Suk San Foong

In Re PATENT APPLICATION Of:

Applicant(s)	:	Yasuo TANAKA	)
Serial No.	:	09/660,484	)
Filed	:	September 12, 2000	) **REQUEST FOR RECONSIDERATION**
		METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE	)
Attorney Ref.	:	OKI 262	)

February 20, 2003

Commissioner for Patents
Washington, D.C. 20231
Box – AF

Sir:

This Request for Reconsideration is filed in response to the final Official Action dated November 20, 2002, the time for response to which is up to and including February 20, 2003. For at least the following reasons, it is respectfully requested that the final rejection of the pending claims be reconsidered and withdrawn.

REMARKS

Claims 3, 7-12 and 14-26 are currently pending in this application. Claims 7-9 are independent claims.

Claims 3, 7-9, 11-12, 14-17 and 19-26 stand rejected under 35 U.S.C. §103(a) as being obvious over Chakravorty, U.S. Patent No. 6,181,569 B1. The rejection is respectfully traversed.

The Examiner relies on the teachings discussed in the rejections of paragraph 12 of the Office Action mailed May 23, 2002. In that previous Action, the Examiner begins with the premise that Chakravorty teaches the method of manufacturing semiconductor device originally recited in claim 1, and now incorporated in independent claims 7-9. The applicant disagrees. The manufacturing method, as

claimed in the present application, recites "placing a sheet of encapsulating material containing a thermosetting resin having a curing temperature over said semiconductor wafer so as to cover said main surface," and "heating and curing said sheet encapsulating material by a heating apparatus to thereby form an encapsulating resin layer." Chakravorty discloses that encapsulation can be done by a number of established approaches such as transfer molding using epoxy resin based mold compounds, laminating with a dry film such as polyimide or other polymeric material, or coating from a liquid solution using techniques such as extrusion, curtain, meniscus, or spin coating (see Chakravorty column 9, line 65, through column 10, line 3). The lamination process disclosed in Chakravorty involves laminating the dry film to the semiconductor wafer using an epoxy adhesive glue (see column 10, lines 29-30), and hence, is not equivalent to the process disclosed in the present application, where no adhesive is required. Moreover, Chakravorty fails to expressly disclose that the encapsulation material used is a thermosetting resin, as the rejected claims require.

In the final Office Action, Response to Arguments, paragraph 4, the Examiner asserts that the claims of the present application "do not exclude use of the adhesive layer of Chakravorty" and "furthermore, Chakravorty discloses that the use of the adhesive layer is optional."

Unfortunately, the Examiner fails to refer to any specific text in Chakravorty in support of his assertion that the adhesive layer is optional. Our own perusal of Chakravorty finds no teaching or suggestion that the dry polymeric film can be used for lamination without the adhesive layer. Chakravorty clearly discloses that "the lamination process is achieved by attaching the laminate film on the wafer by using an adhesive glue under application of pressure and heat" (column 10, lines 34-37). Chakravorty also discloses that " the polymeric film softens under heat and pressure and thus could be made to deform adequately and laminate satisfactorily to the bumped regions providing satisfactory encapsulation" (column 10, lines 43-45). However, there is no disclosure in Chakravorty that the polymeric film undergoes a curing process as a result of the applied heat and pressure, as independent claims 7-9 would require. In the claimed invention, the sheet of encapsulating material is heated and cured after being placed over the main surface of the semiconductor wafer, thus advantageously

encapsulating the main surface without the need for a separate adhesive. It is respectfully submitted that this distinguishing feature is neither taught nor suggested by Chakravorty.

Further, claims 7-9 each recite that the heating and curing step be done in such a manner that the heating of the sheet encapsulating material is at a heating temperature lower than the curing temperature of the sheet encapsulating material, at which the viscosity of the sheet encapsulating material is low and voids contained in the sheet encapsulating material can escape, and that the sheet encapsulating material be kept at the heating temperature for a period of time determined to be sufficient for the voids to be eliminated. It is respectfully submitted that neither Chakravorty nor Gilleo teach or suggest that the curing process includes maintaining the encapsulating material at a heating temperature less than the curing temperature for a period of time, during which the viscosity of the encapsulating material will be low and any voids in the encapsulating material will be able to escape.

In fact, the Examiner fails to point out anything in the references that discusses the problem of voids in the encapsulating material, or a process by which they may be eliminated. In the Office Action of May 23, 2002, the Examiner simply argued that the heating step recited in claims 7 and 8 would be performed during the process of heating the resin to the curing temperature. The applicant disagrees and respectfully submits that there is nothing in the processes disclosed in the prior art references to suggest the claimed benefits of maintaining a temperature below the curing temperature for a period of time. On the contrary, without such suggestion, it would appear that the reasonable course of action for one of ordinary skill in the art would be to raise the temperature as quickly as possible to the cure temperature in order minimize process time.

In the final Office Action, paragraph 6, the Examiner argues in rebuttal that it is implicit in the teachings of Gilleo that a working device is formed that has a sufficiently low quantity of voids such that the device has satisfactory performance. Therefore, the Examiner continues, the rise time to the curing temperature has been determined to be sufficient for the voids to be eliminated. The Examiner argues that alternatively, the choice of rise-time to the curing temperature would have been a matter of routine optimization to achieve a desired thermal budget and its associated cost for the heating

step. The Examiner asserts that the claim does not require a particular duration for the heating step.

As best understood, the Examiner's argument is that the elimination of voids is an inherent part of the process of heating and curing the sheet encapsulating material, as disclosed in the applied references. However, as indicated in MPEP §2112, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to established inherency of that result or characteristic. The Examiner has failed, it is respectfully submitted, to provide a convincing argument the simple heating and curing of the encapsulating materials disclosed in the applied references necessarily achieves the same beneficial result as the process recited in claims 7-9, namely, that the sheet encapsulating material be kept at the heating temperature for a period of time determined to be sufficient for the voids to be eliminated. While it is possible some reduction in voids might result incidentally from the heating and curing processes describes in Chakravorty and Gilleo, there appears to be nothing in these processes that would inherently lead to the elimination of voids, as claimed.

Further, the applicant disagrees with the Examiner's assertion that the claims do not require a particular duration for the heating step. The recited period of time in the claims is "a period of time determined to be sufficient for the voids to be eliminated." Is respectfully submitted that this is a functional limitation, and that the required time could be readily determined by experimentation with the plastic materials to be used, and hence is not indefinite (see MPEP §2173.05(g)).

With regard to the step of heating the encapsulating material at reduced pressure recited in claims 8 and 9, the Examiner took official notice in the Office Action of May 2, 2003, that it was known at the time of the applicant's invention to coat a semiconductor substrate having bump electrodes with resin at a reduce pressure followed by raising the pressure to achieve uniform coating including reduction of voids. The Examiner provided no references, affidavit or other documentation in support of this finding. Similarly, the Examiner failed to provide support for the official notice taken regarding claim 14, that the use of sheet encapsulating material containing a curing agent enclosed in a capsule to broken at a curing temperature was known prior to applicant's invention, or for the official notice taken regarding claim 15, that a sheet

encapsulating material containing an antifoaming agent for removal of voids was known prior to applicant's invention.

The Examiner, citing MPEP §2144.03, asserts in paragraph 8 of the final office Action that it is not necessary to provide a reference at the time of taking Official Notice. While this may be true, §2144.03 also requires that the Examiner cite references in support of his or her position if the applicant traverses the Official Notice. Even though applicant's response on August 23rd, 2002 challenged the Examiner's Official Notice, the Examiner has thus far not provided appropriate support for the assertions made in the Office Action of May 23, 2002, in accordance with the MPEP.

Accordingly, it is respectfully submitted that the Examiner has not met the burden of establishing a prima facie case of obviousness with regard to claims 3, 7-9, 11-12, 14-17 and 19-26, and that the rejection of these claims should be withdrawn.

Claims 10 and 18 stand rejected under 35 USC §103(a) as being obvious over Chakravorty as applied to claims 3, the 7-9, 11-12, a 14-15, and further in view of Gilleo et al., U.S. Publ. No. 20010003058. The rejection is respectfully traversed.

It is respectfully submitted that claims 10 and 18 patentably distinguishes over the applied art combination for at least the reasons discussed above in regard to their respective base claims, claims 7 and 8.

Moreover, it is submitted that claims 7 and 8 independently distinguish over the applied art combination. In rejecting claims 7 and 8, the Examiner relies upon Gilleo for the teachings discussed in the rejection of paragraph 11 of the Office Action mailed on May 23, 2002. In the earlier Office Action, the Examiner argued, with respect to claims 10, that it is inherent that the sheet would not contact the wafer at all points at the same time due at least to local thickness variations in the encapsulant sheet and the topography of the wafer. Alternatively, argued the Examiner, the disclosure of placing the encapsulant sheet would suggest to one of ordinary skill in the art, successively placing the sheet because of the limited number of methods are placing the sheet encompass by the disclosure placing the sheet discussed above in Gilleo (see MPEP §2131.02 and §2144.08).

From the arguments advanced by the Examiner, it appears that the meaning of the claim language is misperceived. It is generally accepted that in interpreting claim

language, reference may be had to the specification. Figure 3 and the text at page 17, line 11 through page 18, line 9 disclose with regard to the method of claims 10 and 18, that the amount of air potentially trapped between the sheet encapsulating material and the bumps-bearing surface of the wafer is reduced by placing the sheet encapsulate material over the wafer so that one edge of the sheet touches one edge of the wafer first, and the rest of the sheet encapsulating material is then progressively brought into contact with the surface of the wafer.

Clearly, the principal argument advanced by the Examiner, namely that it is inherent that the sheet would not contact the wafer at all points at the same time due at least to local thickness variations in the encapsulant sheet and the topography of the wafer, does not address the method recited in claims 10 and 18 for minimizing air trapped in the process of applying the encapsulating sheet material to the wafer surface. Essentially, the Examiner's alternative argument is that the method of applying the sheet encapsulating material recited in claims 10 and 18 is simply a species of the generic application process described in the reference (applying the coating composition to the wafer, Gilleo paragraph 0028) and would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made. However, it is respectfully submitted that the method recited in claims 10 and 18 is not one of those application methods that could be envisioned by one of ordinary skill in the art based on the disclosures in the prior art references taken as a whole (see MPEP §2131.02). The essential detail of applying encapsulation material starting at one edge of the wafer, is nowhere suggested in the references.

Moreover, Gilleo is not even really directed to an encapsulation technique, but rather to a technique for applying an integrated flux and underfill material to a flip chip having solder bumps. Given the major differences in structure and function between the two inventions, is respectfully submitted that one of ordinary skill in the art would not have been motivated to combining to references in the matter proposed by the Examiner.

For these reasons, it is submitted that claims 10 and 18 independently distinguish over the applied art references, whether taken individually or combination.

In summary, it is submitted that this application is in condition for allowance.

Such action, and the passing of this case to issue are respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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